**EE 465 Lab Report**

*Lab 2 – Standard Cell Design*

Written by: Anh Q. Ho

Lab Section – Monday 04:10pm

Abstract

Standard cells are the basic cells which widely used in digital design. They consists of basic logic gates, buffers, D-flip flop, multiplexers, and even half and full adders. The performance of the standard cells determines the performance of the circuit to a large extent. The objective of this lab is to have students to get a hands-on experience with the knowledge of EE 330.

Introduction

In this lab, students are to build a standard cell, DFF with Cadence Virtuoso and will learn about the standard cell characterization in next lab. So the requirements for this lab are to have the layout and schematic and DRC testing successful, below shows the steps to meet the requirement.

Result:

1. Building schematic
2. Drawing and layout
3. LVS and DRC testing

The design of the DFF is given below:

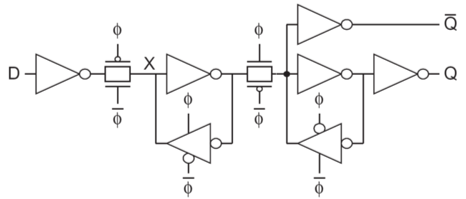


Figure -DFF design

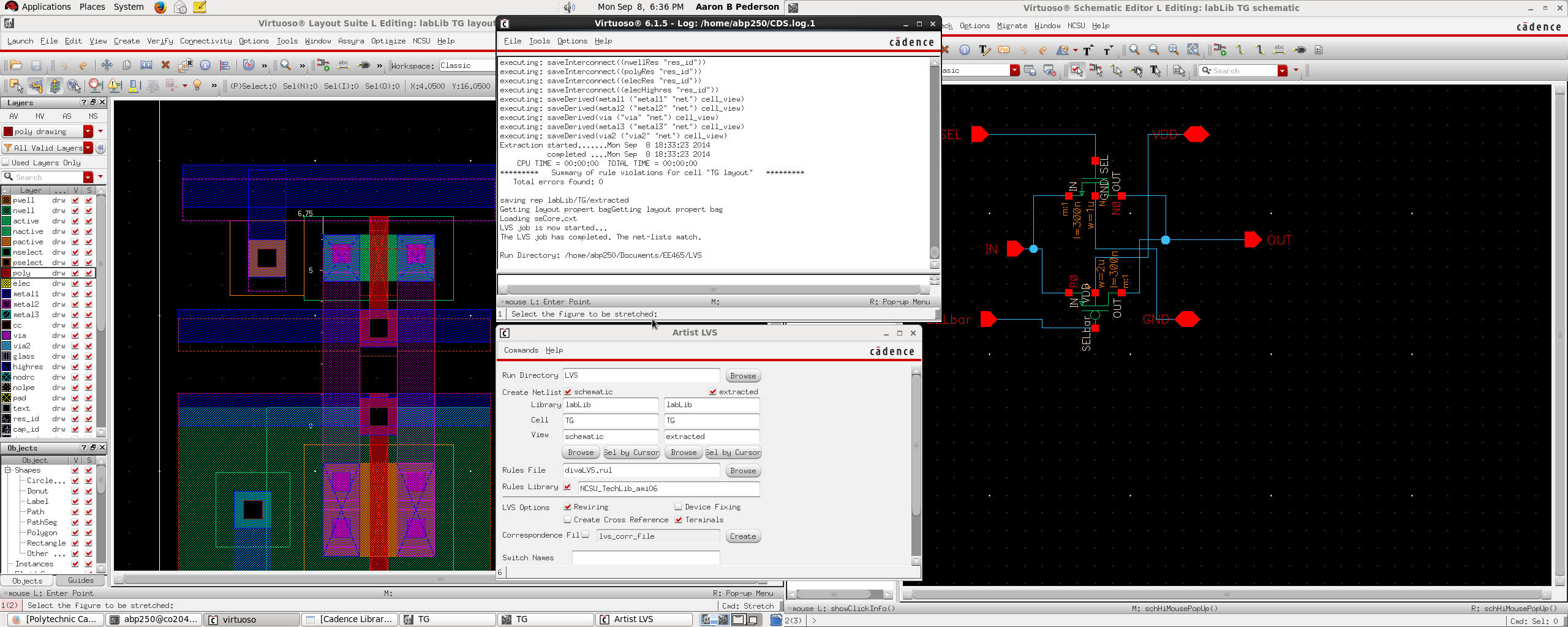
results & Discussion

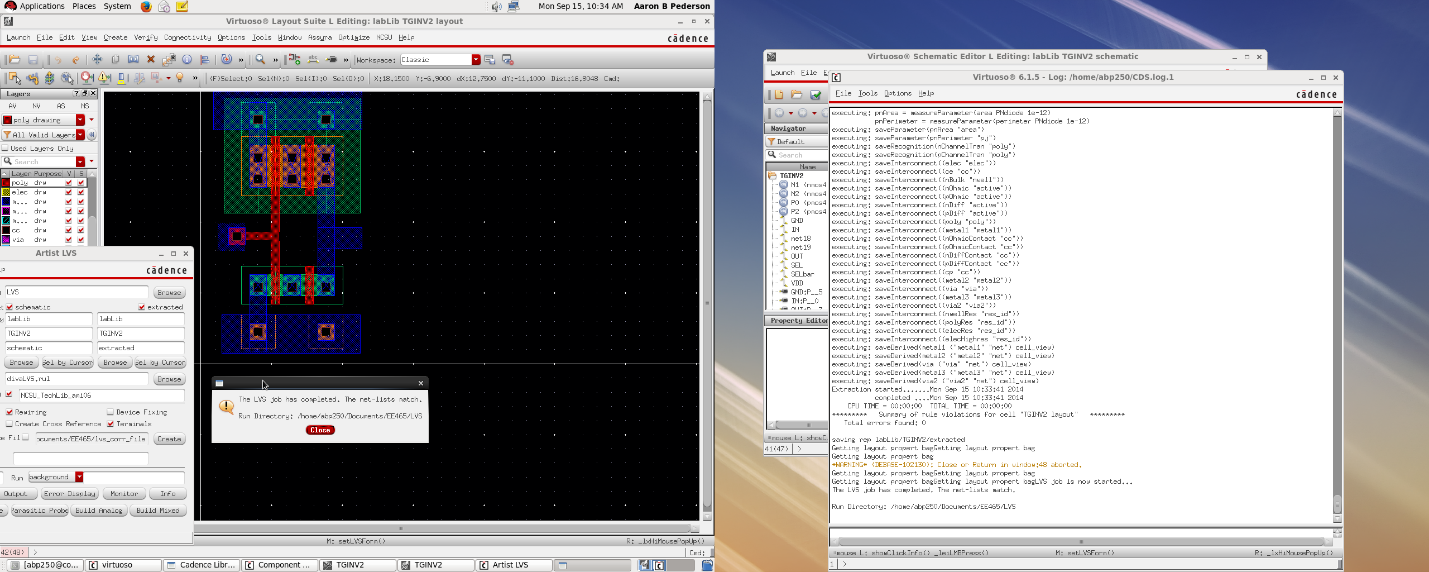
Figure -LVS result of the transmission gate. 

Figure -LVS and DRC results of the tri-gate inverter.

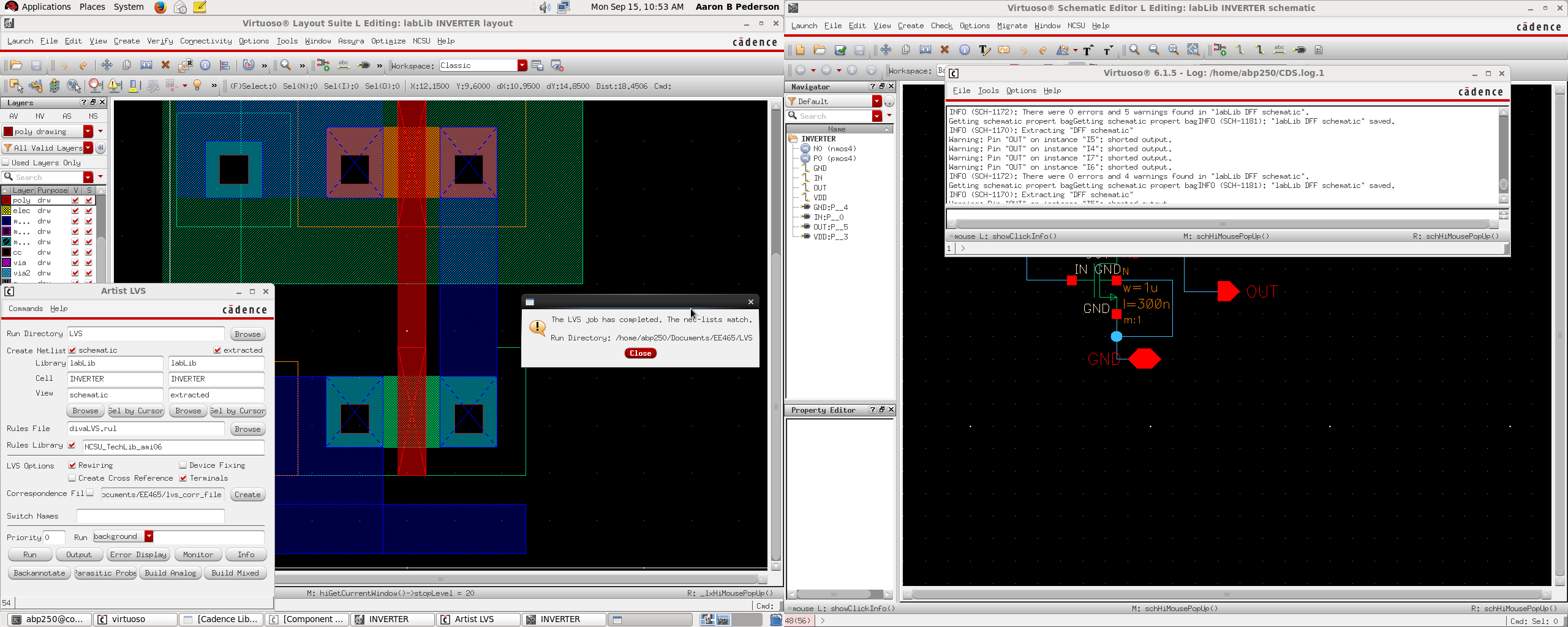


Figure -Inverter LVS and DRC results

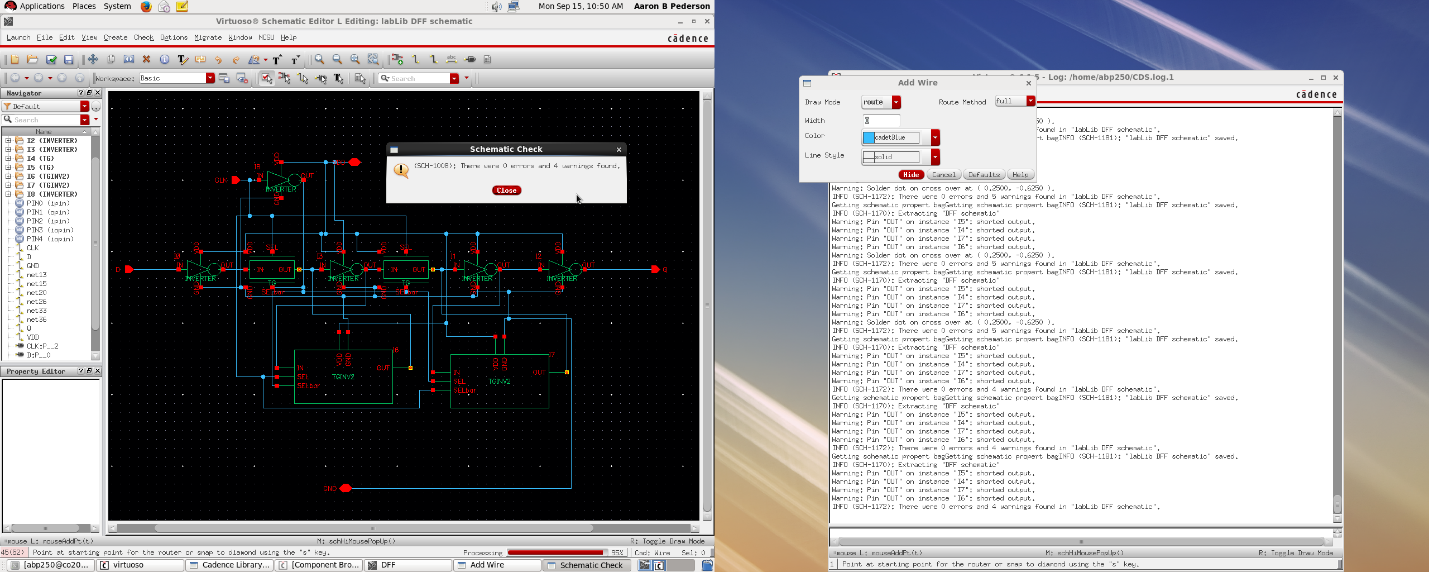


Figure -Circuit schematic of the standard cell.

According to the, LVS and DRC results of three main components (Inverter, Transmission Gate, and Tri-gate Inverter), the requirement are met, but the circuit schematics has 4 warnings (0 errors), but were unable to determine the problem. So, maybe the problems may get taken care of when the graphical analysis is done (week 3 lab).

Conclusion

This lab went fairly well, the main problem for the group is to define the schematic of the transmission gate and tri-gate inverter. As a group, the other difficulty is the 4 warnings on the standard cell circuit schematic during the DRC testing and unable to explain the problem.